BPM Electronics and Signal Processing

FETS Meeting 17-04-2013

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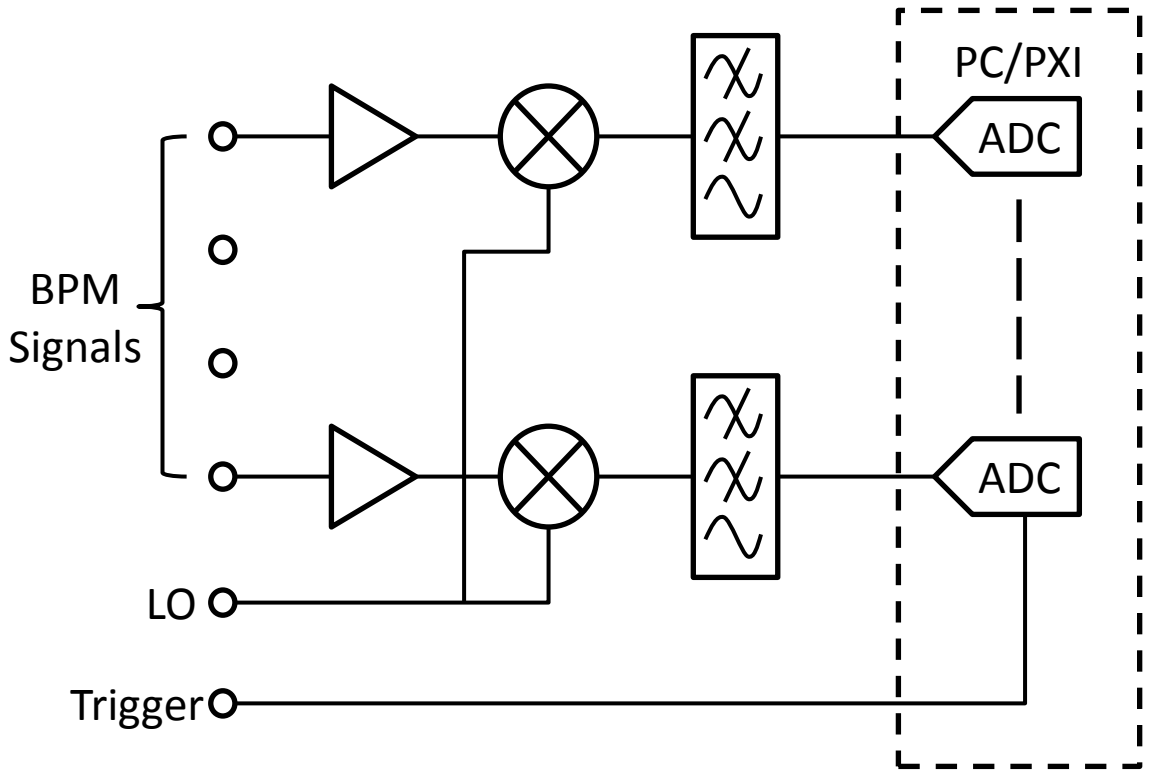
BPMs

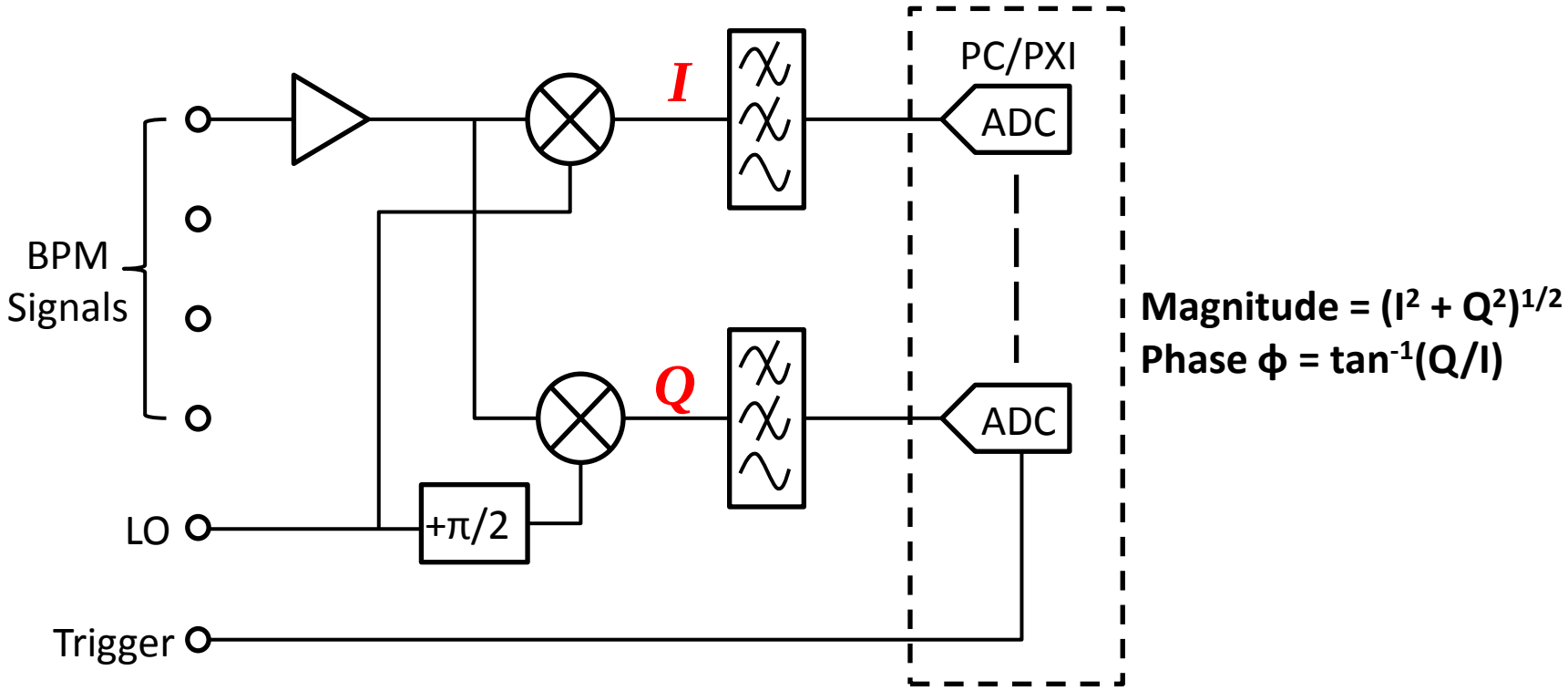
- Six BPMs (maximum) foreseen
- Obtain beam position with 0.1mm resolution and 0.1mm accuracy
- Post-chopper fast BPM direct to fast scope (no processing)
- Phase measurement required (Alan)
- Aim is to produce a BPM system that has the best performance for the least cost

Magnitude only



Each electrode is mixed to an IF of 10MHz, sampled at 50MS/s, split into ‘segments’, max and min of each segment found, maxes and mins meaned, difference/sum position calculated

I/Q down-conversion in electronics



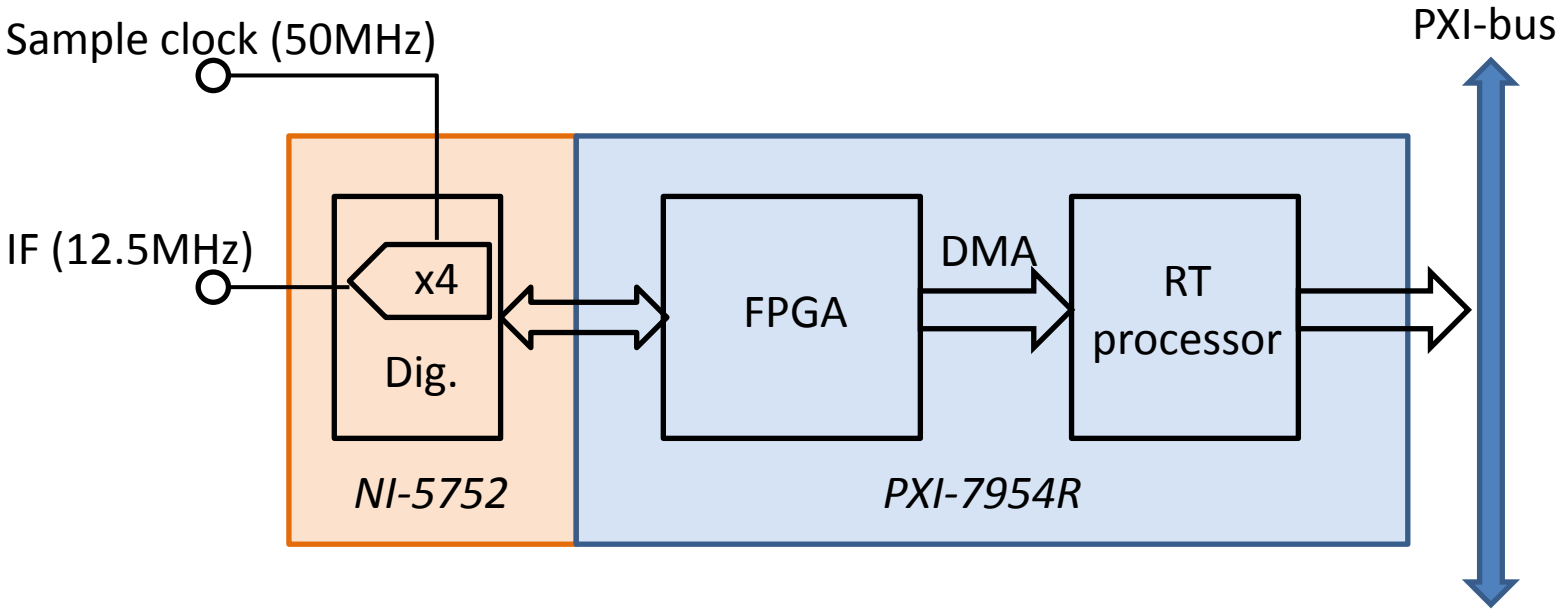
Can create both I and Q in electronics and use two digitizer channels to sample. Accurate but inefficient use of digitizer. I/Q results more accurate than I-only

LINAC4 front-end electronics

- LINAC4 BPM front-end electronics will do the job (subject to IF and gain tweaks)
- Richard had discussion with Jocelyn Tan about using a LINAC4 card
- Design is already developed and debugged
- Based on 6U format (VME) card – RHUL has spare VME sub-racks for cards

I/Q in FPGA & RT Processor

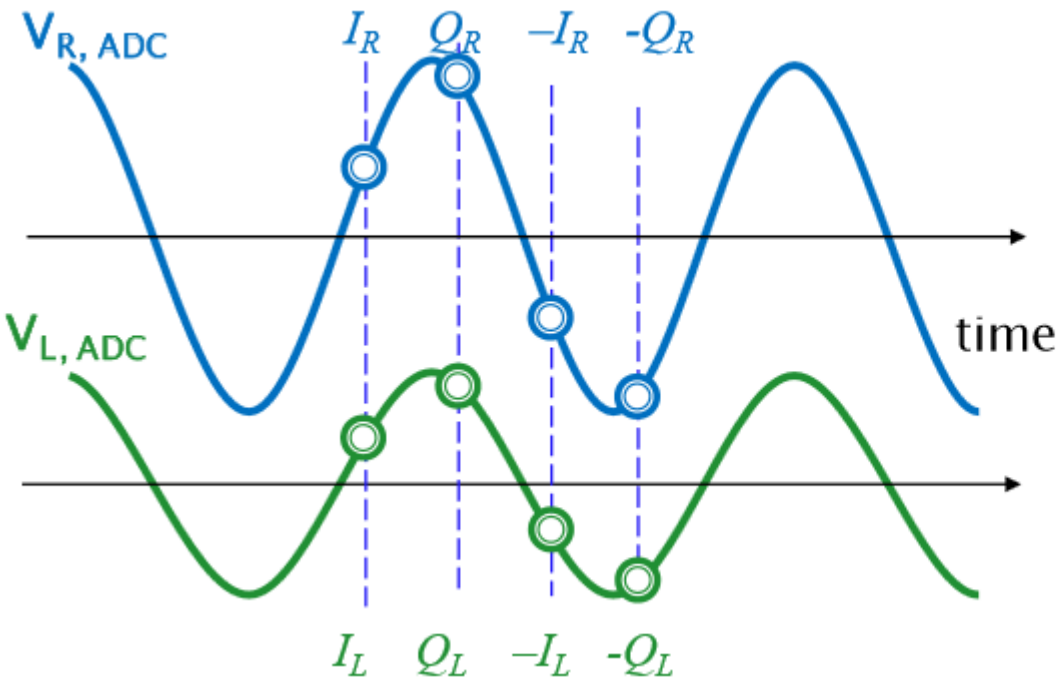
- Obtain I in electronics; sample in one channel; get Q in FPGA code
- Sample at four times IF – sample N (I) is equivalent to sample N-1 as Q
- Code being developed for FPGA and RT processor to test
- Requires sampling clock locked to bunch RF



Signal Processing

Magnitude = √ ($I^2 + Q^2$)

Phase ϕ = $\tan^{-1}$ (Q/I)



$$\Delta x = \frac{M_R - M_L}{M_R + M_L + M_U + M_D}$$

$$\varphi = \varphi_{beam} - \varphi_{LO}$$

$$I = M_R + M_L + M_U + M_D$$

$$TOF = \varphi_{PU2} - \varphi_{PU1}$$

(From Jocelyn Tan, Linac4 Instrumentation Review 18th October 2011)

I/Q - Implications

- Each BPM uses four channels – selected digitizer has 32 channels
- Position resolution and error improved with I-Q, rather than I-only
- Phase information comes at no extra cost
- Sample at integer multiple of intermediate frequency (IF) – digitizer samples at 50MHz, so mix to 10MHz or 12.5MHz (multiple of four requires less maths than five! → easier in an FPGA)
- BUT requires sample clock phase-locked with bunch RF
- This requires an LO that can be externally referenced

Updated Costs

FPGA/Digitizer (extra discount from NI, largest FPGA)	£9.9k
Front End - connectorised	£1.3k each
Front End - LINAC4	£0.5k each
Local Oscillator distribution (not LO)	£0.6k
Front End power (only for connectorised FE)	£0.5k
Cabling, connectors for 6 BPMs/front ends	£1.4k
Miscellaneous (racks, patch panels)	£0.3k
TOTAL (6 BPMs, connectorised FE)	**£20.5k**
TOTAL (6 BPMs, LINAC4 FE)	**£15.2k**

Costs estimated to within 5-10%

Work still to do…

- BPM Wiki page section update
- Calculate resolution of I/Q measurement in FPGA vs HW I/Q
- FPGA code – test with more segments, partitioning of FPGA/RT code, max number of BPMs etc
- Decide on connectorised vs LINAC4 front-end electronics (phone meeting next week with JT to discuss LINAC4 card further)
- Organise purchasing arrangements
- Design calibration/testing jig