BPM Processing Meeting 29-01-2013 - Minutes

Richard D'Arcy, Simon Jolly, Gary Boorman

Objective

To obtain relative costs/timescales for various BPM signal processing options.

1. **BPM Hardware**
    - **a.** Four 'slow' (324MHz) and one 'fast' (after chopper to measure shortened pulses).
    - **b.** BPM type: probably use LINAC4 shortened-stripline designed for 352MHz. This has been shown to work at 202MHz at LINAC2. Getting information from CERN is proving difficult - ***RD*** to contact Rhodri and obtain BPM specs (signal levels etc). This is the preferred BPM solution.
    - **c.** Bergoz sell BPMs and processing items – ***GB*** to contact Bergoz for details and prices. Use commercial BPMS if the CERN ones aren't forthcoming.
    - **d.** A self-made BPM design is possible, but is a lengthy process. Juergen and Pete appear to be investigating this route.
    - **e.** ***RD*** will contact Manfred Wendt and Vic Scarpine at Fermilab to get specs of the PXIE BPMs.
    - **f.** 100µm resolution sufficient.
2. **BPM Signal Processing**
    - **a.** 12.5GSa/s Scope to view fast BPM already exists. ***Saad Alsari*** is the person to contact.
    - **b.** One Tektronix DPO4034B (or equivalent) to be purchased to view slow BPM signals directly. Cost £7250 (15% off list price from Farnell, could perhaps do better) and already on shopping list. ***Who*** is buying?
    - **c.** Homodyne system (324MHz LO) with splitter and LP filter to reduce noise above 324MHz (which may be aliased). 16 channels required. Splitting of the LO to each channel required. ***GB*** to provide outline electronics design and cost estimate.
    - **d.** Each channel to be digitized at several 10s of MSa/s using PXI-based system.
        - **i.** DAQ card can acquire data and move it along the PCI backplane to the processor card to do the position maths.
        - **ii.** FPGA card with DAQ front-end. Position calculations split between the FPGA and RT processor before much-reduced data being moved to processor card. ***GB*** to investigate how much FPGA and RT processor power required; ***GB*** to get cost estimate of FPGA & FE card.
    - **e.** Position information served via EPICS IOC on PXI processor card.
    - **f.** EPICS Clients – logging program for all server data; console viewer for last *N* BPM positions; experiments to grab relevant data.

g. *Not discussed:* testing the completed electronics, using calibration tone – requires injection (using coupler) into BPM signal path.
h. Cost estimate for all processing: electronics is roughly £5k; FPGA +DAQ £8-10k; scope £7k. This allows about £20k for BPMs. ***GB*** to determine costs.

3. **General DAQ**
   a. Two PCs required: one for logging all data and console viewer; one for 'experimental' work. Budget £4k.
   b. Determine suitable datafile formats and interfaces for IOCs. ***GB***
   c. PXI system can also distribute precision triggers and clocks, since it has relevant cards already within the system.
4. **Next FETS Meeting (13th Feb)**
   a. GB can't make meeting due to DESY commitment. ***GB*** to prepare slides of processing design, cost and schedule. ***SJ*** or ***RD*** to present.