BPM Processing Options
FETS Meeting 13-03-2013

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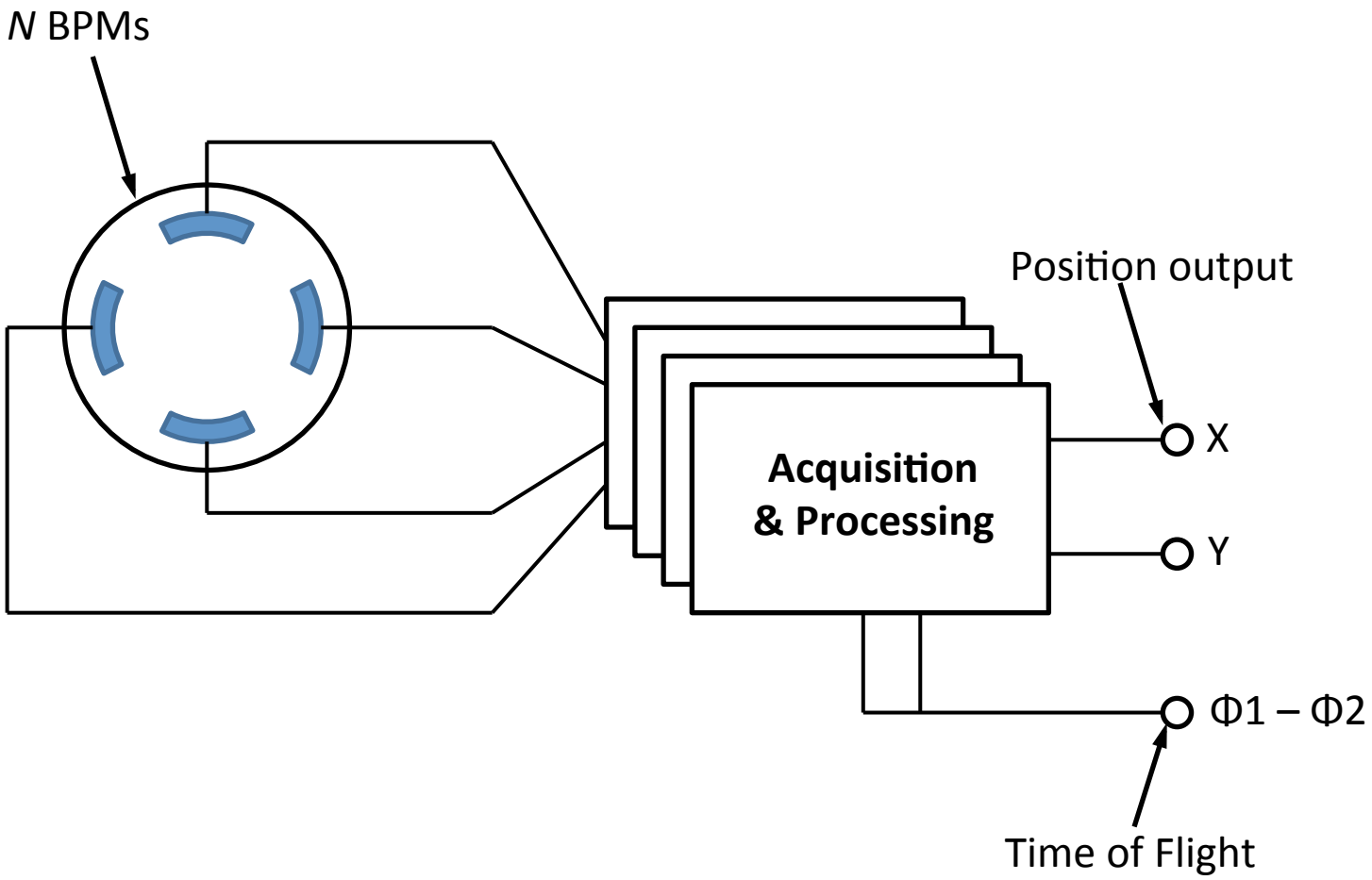
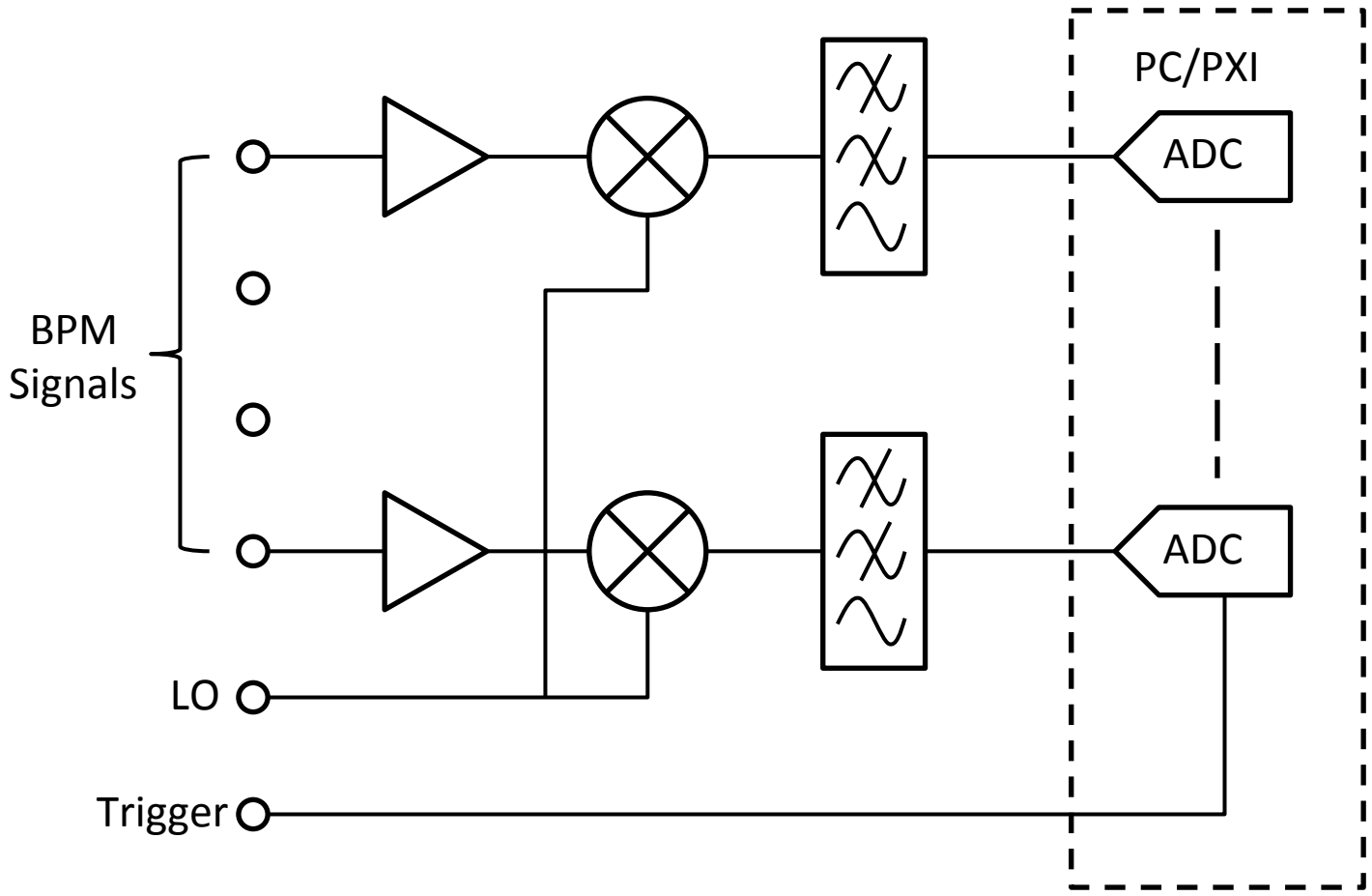
BPM Processing



BPM Processing – Down Conversion and DAQ



BPM Processing – Down-Conversion

- **Bergoz (BPM-AFE) card**
  - Four Channels (one BPM); IF 10-100MHz
  - Includes Calibration Tone input; no 'raw' signal output
  - Balanced signal out (ground loop elimination)
  - Cost: £1.8k per card, but requires some mounting hardware (~£500)
  - Delivery time 14 weeks ARO
- **Self-made Connectorised Front-End**
  - Use connectorised elements from Hititte, Mini-circuits etc
  - Join elements using SMA connectors and RG174 cable
  - Easy testing and development
  - Requires some design effort
  - Cost ~£1.3k per BPM
- **Self-made RF PCB**
  - Use RF IC components
  - Compact and cheap £200-300 per BPM
  - Long design and testing schedule, but could base design on connectorised version above
- Each option requires some hardware such as 19" boxes, control signals etc

BPM Processing – DAQ/Digitizing Options

- **Data Acquisition Cards**
  - Acquire at tens of MS/s per channel within PXI system
  - Move data to PXI processor card and obtain position
  - Resultant positions served via IOC
  - Cost £4k per eight channels (4 per BPM) eg PXI-5105, 12-bit
- **Digitizer and FPGA**
  - Use FPGA with Digitizer front-end within PXI system
  - Digitizer 50MS/s 32 channel (diff), 12-bit, simultaneous sample
  - Can do processing within FPGA and pass result to processor and serve via IOC
  - PXI-based FPGA card with breakout box
  - Cost £7-10k, depending on FPGA size required (work is ongoing) including digitizer, FPGA, breakout box, cable
  - Very fast position calculation
- **'Slow' Oscilloscopes**
  - Could digitize using a low BW scope
  - Have to move data across network at 40MByte/s for four BPMs! This will seriously load gigabit ethernet – not recommended!
  - Cost £4-8k depending on scope selected.

Digitizer and FPGA

- 50MS/s 32-channel digitizer; ENOB about 10.7 bits
- Most accurate measurement uses I-Q , or 8 channels per BPM
- Digitizer clock jitter ~8ps
- Easy synchronisation of digitizer clock with LO
- Can borrow a system from NI to test
- If 6 BPMs with I-Q in use will require two Digitizer/FPGA cards

Cost

FPGA/Digitizer, depending on results of testing	£7-10k
Front End (Connectorised)	£1.3k each
Local Oscillator distribution (not LO)	£0.6k
Front End power	£0.5k
Cabling, connectors for 6 BPMs/processors	£1.4k
Miscellaneous (racks, patch panels)	£0.3k
TOTAL (6 BPMs, only one FPGA/Digitizer card)	**£17.5-20.5k**

Costs estimated to within 5-10%

BPM Processing – Summary

- How many BPMs actually used? Design for five or six BPMs…
- Could use Linac4 design (or indeed hardware) for front-end?
- Recommend connectorised front end with PXI Digitizer/FPGA
- Cost could be reduced by £*few* k: develop/test connectorised front-end, then transfer to PCB. Takes extra few weeks
- Work on simulating front-end and FPGA ongoing, but basic design done
- Resolution of 0.1mm should be achievable
- Calibrating the BPMs – use Beadpull setup at RHUL with summer student