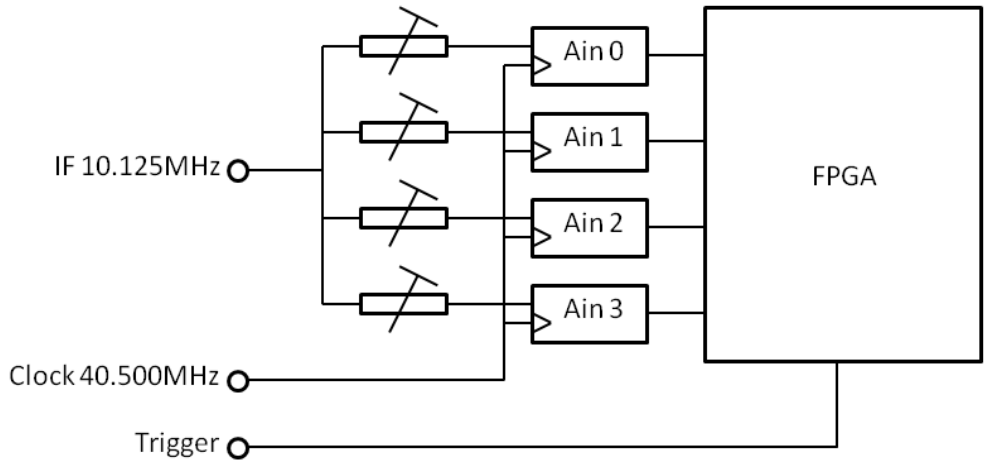
FEST BPM Testing

G Boorman 5th September, 2013

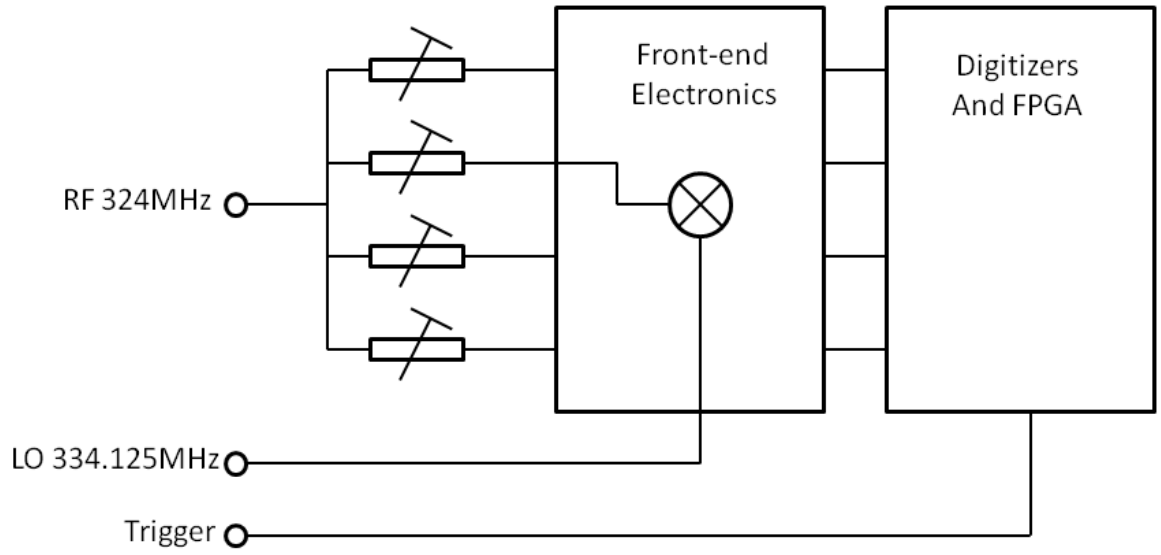
The processing elements of the FETS BPM can be tested before the FETS BPMs are installed in a working beamline. An outline of each stage is testing is described.

1) Digital Processing



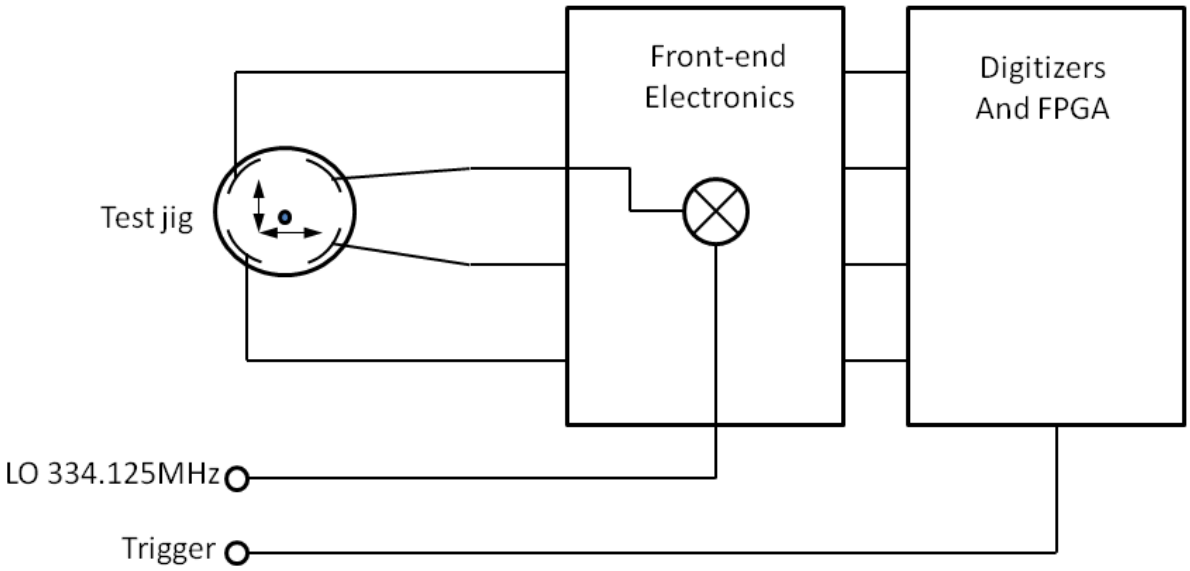
Use an RF source at 10.125MHz, with a splitter and variable attenuation to test the acquisition and FPGA processing. Ensure signals are no greater than 2V peak-to-peak. The clock source is a TTL signal, as is the trigger.

2) Front-end Electronics



The RF is 324MHz and will emulate the signals from the BPM. The LO should be 10.125MHz different from the RF, either above or below. The LO is either 31/32 x RF, or 33/32 xRF.

3) Using the CERN BPM Test-jig



The test-jig uses a movable wire within the BPM, carrying a current with frequency of 324MHz. The LO are trigger are the same as the electronics test.

For each test the RF, LO and clock source generators should be linked using a 10MHz reference as found on most reasonable test equipment, to ensure phase locking of the IF and clock source.